240pin Unbuffered DDR3 SDRAM MODULE

Based on 128Mx8 DDR3 SDRAM A Die

Features

• Performance:

Speed Sort		PC3-8500	PC3-10660	PC3-12800	Unit
		-BE	-CG	-DG	
DIMM $\overline{CAS}$ Latency		7	9	9	
f_{CK}	Clock Frequency	533	667	800	MHz
t_{CK}	Clock Cycle	1.875	1.5	1.25	ns
f_{DQ}	DQ Burst Frequency	1066	1333	1600	Mbps

• JEDEC Standard 240-pin Dual In-Line Memory Module
• 128Mx64 and 256Mx64 DDR3 Unbuffered DIMM based on 64Mx8 DDR3 Elixir SDRAM
• Intended for 533MHz, 667MHz and 800MHz applications
• Inputs and outputs are SSTL15 compatible
• $V_{DD} = V_{DDQ}$ = 1.5Volt ± 0.075Volt
• SDRAMs have 8 internal banks for concurrent operation
• Differential clock inputs
• Data is read or written on both clock edges
• 8 bit pre-fetch
• Two different termination values (Rtt_Nom & Rtt_WR)
• Extended operating temperature rage
• Auto Self-Refresh option
• Automatic and controlled precharge commands
• Programmable Operation:
  - DIMM $\overline{CAS}$ Latency: 5,6,7,8,9,10
  - Burst Type: Sequential & Interleave
  - Burst Length: BC4, BL8
  - Operation: Burst Read and Write
• 14/10/1 Addressing (row/column/rank) – 1GB
• 14/10/2 Addressing (row/column/rank) – 2GB
• Serial Presence Detect
• Gold contacts
• SDRAMs in 78 FBGA Package
• RoHS and Halogen-Free compliance

Description

M2F1G64CB88A4N and M2F2G64CB8HA4N are 240-Pin Double Data Rate 3 (DDR3) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM), organized as one-rank 128Mx64 and two ranks 256Mx64 high-speed memory array. M2F1G64CB88A4N uses eight 128Mx8 DDR3 SDRAMs. M2F2G64CB8HA4N uses sixteen 128Mx8 DDR3 SDRAMs. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All Elixir DDR3 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

The DIMM is intended for use in applications operating up to 533 MHz (667MHz or 800MHz) clock speeds and achieves high-speed data transfer rates of up to 1066Mbps (1333 Mbps or 1600 Mbps). Prior to any access operation, the device $\overline{CAS}$ latency and burst / length / operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0, BA1, and BA2 are using for the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Leads	Power	Note
M2F1G64CB88A4N-BE	533MHz (1.875ns@ CL = 7)	DDR3-1066	PC3-8500	128Mx64	Gold	1.5V	
M2F1G64CB88A4N-CG	667MHz (1.5ns@ CL = 9)	DDR3-1333	PC3-10660				
M2F1G64CB88A4N-DG	800 MHz(1.25ns@ CL = 9)	DDR3-1600	PC3-12800				
M2F2G64CB8HA4N-BE	533MHz (1.875ns@ CL = 7)	DDR3-1066	PC3-8500	256Mx64			
M2F2G64CB8HA4N-CG	667MHz (1.5ns@ CL = 9)	DDR3-1333	PC3-10660				
M2F2G64CB8HA4N-DG	800 MHz(1.25ns@ CL = 9)	DDR3-1600	PC3-12800				

Pin Description

Pin Name	Description	Pin Name	Description
A0-A13	Address Inputs	SCL	Serial Presence Detect Clock Input
BA0–BA2	SDRAM Bank select	SDA	Serial Presence Detect Data input/output
$\overline{RAS}$	Row Address Strobe	SA0-SA2	Serial Presence Detect Address Inputs
$\overline{CAS}$	Column Address Strobe	V_{DD}	SDRAM core power supply
$\overline{WE}$	Write Enable	V_{DDQ}	SDRAM I/O Driver power supply
$\overline{S0}$, $\overline{S1}$	Chip Selects	V_{REFDQ}	SDRAM I/O reference supply
CKE0-CKE1	Clock Enable	V_{REFCA}	SDRAM command/address reference supply
ODT0-ODT1	On die termination control lines	V_{SS}	Ground
DQ0-DQ63	Data input/output	V_{DDSPD}	Serial EEPROM positive power supply
DQS0-DQS7 $\overline{DQS0}$-$\overline{DQS7}$	SDRAM differential data strobes	NC	No Connect
DM0-DM7	Input Data Mask/High Data Strobes	V_{TT}	SDRAM I/O termination supply
CK0-CK1, $\overline{CK0}$-$\overline{CK1}$	Differential Clock Inputs	$\overline{RESET}$	Set DRAMs to Know State
Note: CK1, $\overline{CK1}$, $\overline{SI}$, OTD1 and CKE1 are used for 2GB module only.			

Pinout

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V_{REFDQ}	42	NC	82	DQ33	121	V_{SS}	162	NC	202	V_{SS}
2	V_{SS}	43	NC	83	□ □V_{SS}□ □	122	DQ4	163	V_{SS}	203	DM4
3	DQ0	44	V_{SS}	84	$\overline{DQS4}$	123	DQ5	164	NC	204	NC
4	DQ1	45	NC	85	DQS4	124	V_{SS}	165	NC	205	V_{SS}
5	V_{SS}	46	NC	86	V_{SS}	125	DM0	166	V_{SS}	206	DQ38
6	$\overline{DQS0}$	47	V_{SS}	87	DQ34	126	NC	167	NC	207	DQ39
7	DQS0	48	NC	88	DQ35	127	V_{SS}	168	$\overline{RESET}$	208	V_{SS}
8	V_{SS}	KEY		89	V_{SS}	128	DQ6	KEY		209	DQ44
9	DQ2	49	NC	90	DQ40	129	DQ7	169	CKE1/NC	210	DQ45
10	DQ3	50	CKE0	91	DQ41	130	V_{SS}	170	V_{DD}	211	V_{SS}
11	V_{SS}	51	V_{DD}	92	V_{SS}	131	DQ12	171	NC	212	DM5
12	DQ8	52	BA2	93	$\overline{DQS5}$	132	DQ13	172	NC	213	NC
13	DQ9	53	NC	94	DQS5	133	V_{SS}	173	V_{DD}	214	V_{SS}
14	V_{SS}	54	V_{DD}	95	V_{SS}	134	DM1	174	A12 / $\overline{BC}$	215	DQ46
15	$\overline{DQS1}$	55	A11	96	DQ42	135	NC	175	A9	216	DQ47
16	DQS1	56	A7	97	DQ43	136	V_{SS}	176	V_{DD}	217	V_{SS}
17	V_{SS}	57	V_{DD}	98	V_{SS}	137	DQ14	177	A8	218	DQ52
18	DQ10	58	A5	99	DQ48	138	DQ15	178	A6	219	DQ53
19	DQ11	59	A4	100	DQ49	139	V_{SS}	179	V_{DD}	220	V_{SS}
20	V_{SS}	60	V_{DD}	101	V_{SS}	140	DQ20	180	A3	221	DM6
21	DQ16	61	A2	102	$\overline{DQS6}$	141	DQ21	181	A1	222	NC
22	DQ17	62	V_{DD}	103	DQS6	142	V_{SS}	182	V_{DD}	223	V_{SS}
23	V_{SS}	63	CK1/NC	104	V_{SS}	143	DM2	183	V_{DD}	224	DQ54
24	$\overline{DQS2}$	64	$\overline{CK1}$/NC	105	DQ50	144	NC	184	CK0	225	DQ55
25	DQS2	65	V_{DD}	106	DQ51	145	V_{SS}	185	$\overline{CK0}$	226	V_{SS}
26	V_{SS}	66	V_{DD}	107	V_{SS}	146	DQ22	186	VDD	227	DQ60
27	DQ18	67	V_{REFCA}	108	DQ56	147	DQ23	187	NC	228	DQ61
28	DQ19	68	NC	109	DQ57	148	V_{SS}	188	A0	229	V_{SS}
29	V_{SS}	69	V_{DD}	110	V_{SS}	149	DQ28	189	V_{DD}	230	DM7
30	DQ24	70	A10/AP	111	$\overline{DQS7}$	150	DQ29	190	BA1	231	NC
31	DQ25	71	BA0	112	DQS7	151	V_{SS}	191	V_{DD}	232	V_{SS}
32	V_{SS}	72	V_{DD}	113	V_{SS}	152	DM3	192	$\overline{RAS}$	233	DQ62
33	$\overline{DQS3}$	73	$\overline{WE}$	114	DQ58	153	NC	193	$\overline{S0}$	234	DQ63
34	DQS3	74	$\overline{CAS}$	115	DQ59	154	V_{SS}	194	V_{DD}	235	V_{SS}
35	V_{SS}	75	V_{DD}	116	V_{SS}	155	DQ30	195	ODT0	236	V_{DDSPD}
36	DQ26	76	$\overline{S1}$/NC	117	SA0	156	DQ31	196	A13	237	SA1
37	DQ27	77	ODT1/NC	118	SCL	157	V_{SS}	197	V_{DD}	238	SDA
38	V_{SS}	78	V_{DD}	119	SA2	158	NC	198	NC	239	V_{SS}
39	NC	79	NC	120	V_{TT}	159	NC	199	V_{SS}	240	V_{TT}
40	NC	80	V_{SS}			160	V_{SS}	200	DQ36		
41	V_{SS}	81	DQ32			161	NC	201	DQ37		

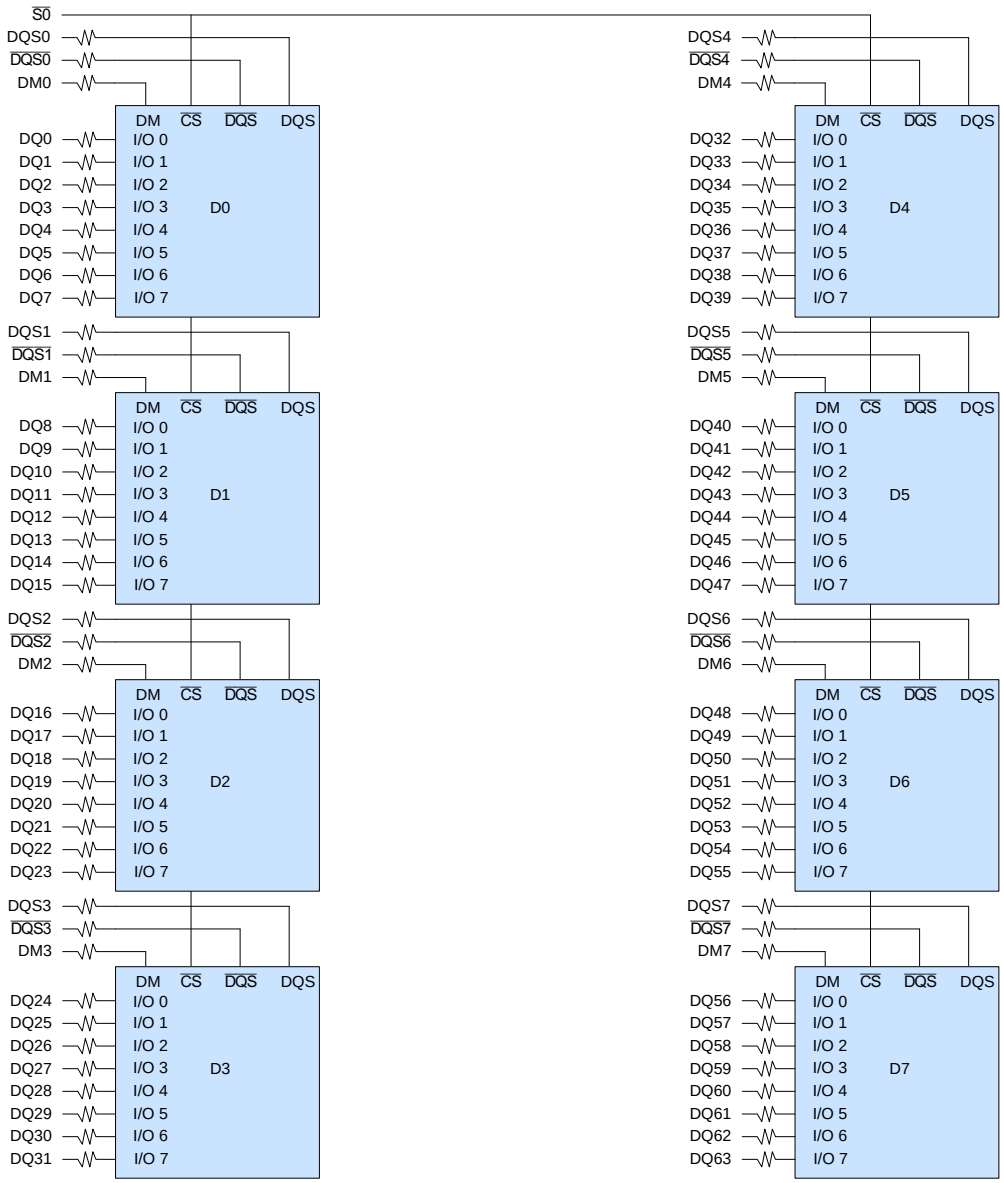
Note:
1. NC = No Connect.
2. Pin 63, 64, 76, 77 and 169 (CK1, $\overline{CK1}$, $\overline{SI}$, OTD1 and CKE1) are used for 2GB module only.

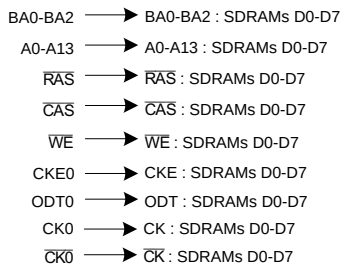
Input/Output Functional Description

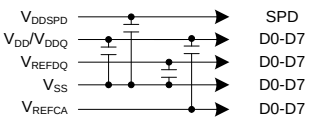
Symbol	Type	Polarity	Function
CK0-CK1 $\overline{CK0}$-$\overline{CK1}$	SSTL	Differential crossing	CK and $\overline{CK}$ are differential clock inputs. All the DDR3 SDRAM address/control inputs are sampled on the crossing of positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is reference to the crossing of CK and $\overline{CK}$.
CKE0-CKE1	SSTL	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{S0}$-$\overline{S1}$	SSTL	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	SSTL	Active Low	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ (along with $\overline{S}$) define the command being entered.
V_{REFDQ}	Supply		Reference voltage for SSTL15 I/O inputs
V_{REFCA}	Supply		Reference voltage for SSTL15 command/address inputs
V_{DDQ}	Supply		Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity.
ODT0-ODT1	SSTL	Active High	When high, termination resistance is enabled for all DQ, DQS, $\overline{DQS}$, and DM pins, assuming this function is enabled in the Mode Register 1 (MR1).
BA0 – BA2	SSTL	-	Selects which SDRAM bank is to be active.
A0 – A13	SSTL	-	During a Bank Activate command cycle, Address input defines the row address (RA0-RA13). During a Read or Write command cycle, Address input defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with B0 and B1 to control which banks(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1, or BA2. If AP is low, BA0, BA1, and BA2 are used to define which bank to precahrge. A12 ($\overline{BC}$) is sampled during READ and WRITE commands to determine if burst chop (on-the –fly) will be performed (High, no burst chop; Low, burst chopped).
DQ0 – DQ63	SSTL	Active High	Data and Check Bit Input/Output pins.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR3 SDRAM input buffers and core logic.
DQS0 – DQS7 $\overline{DQS0}$ – $\overline{DQS7}$	SSTL	Differential crossing	Data strobe for input and output data.
DM0 – DM7	Input	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loadings.
SA0 – SA2		-	These signals are tied at the system planar to either Vss or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A external resistor must be connected from the SDA bus line to V_{DD} to act as a pull-up on the system board.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pull-up.
V_{DDSPD}	Supply		Power Supply for SPD EEPROM. This supply is separate from the VDD/VDDQ power plane. EEPROM supply is operable from 3.0V to 3.6V.

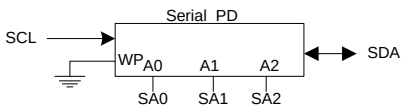
Functional Block Diagram

(1GB, 1 Rank, 128Mx8 DDR3 SDRAMs)



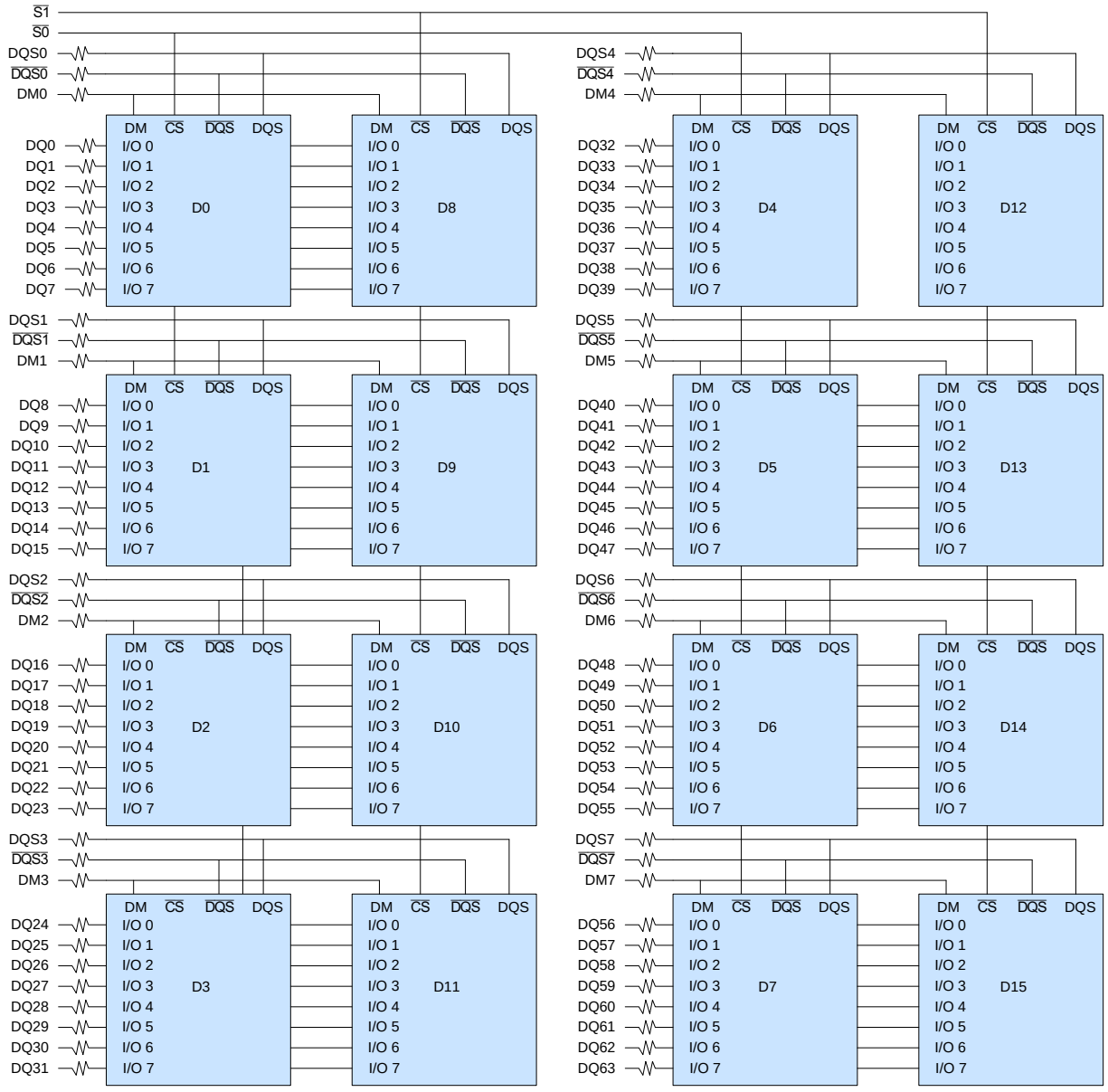


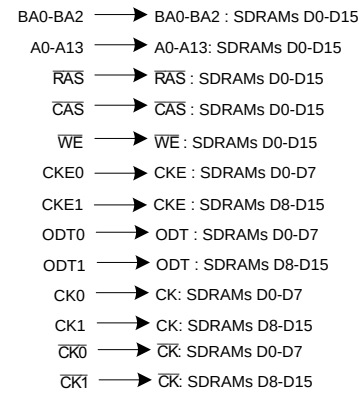


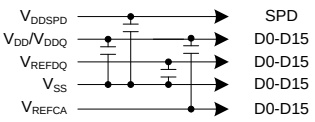


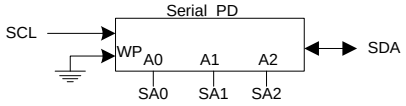
Functional Block Diagram

(2GB, 2 Rank, 128Mx8 DDR3 SDRAMs)









Serial Presence Detect -- Part 1 of 2 (1GB)

128Mx64 1 Rank UNBUFFERED DDR3 SDRAM DIMM based on 128Mx8, 8Banks, 8K Refresh, 1.5V DDR3 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		-BE	-CG	-DG	-BE	-CG	-DG	
0	CRC range, EEPROM bytes, bytes used	CRC Covers Bytes: 0~116, Total SPD Bytes: 256, SPD Bytes Used: 176,			92			
1	SPD revision	Revision 0.8			08			
2	DRAM device type	DDR3 SDRAM			0B			
3	Module type (form factor)	UDIMM			02			
4	SDRAM Device density and banks	8 banks, 1Gb			02			
5	SDRAM device row and column count	14 rows, 10 columns			11			
6	Reserved	Undefined			00			
7	Module ranks and device DQ count	1 ranks, 8 bits			01			
8	ECC tag and module memory Bus width	Non ECC, 64bits			03			
9	Fine timebase dividend/divisor (in ps)	2.5ps			52			
10	Medium timebase dividend	1ns			01			
11	Medium timebase divisor	8ns			08			
12	Minimum SDRAM cycle time (tCKmin) (ns)	1.875	1.5	1.25	0F	0C	0A	
13	Reserved	Undefined			00			
14	CAS latencies supported	6,7,8	6,8,9	5,6,7,8,9,10	1C	34	7E	
15	CAS latencies supported	Undefined			00			
16	Minimum CAS latency time (tAAmin) (ns)	13.125	13.5	11.25	69	6C	5A	
17	Minimum write recovery time (tWRmin)	15ns			78			
18	Minimum $\overline{\text{CAS}}$-to-$\overline{\text{CAS}}$ delay (tRCDmin) (ns)	13.125	13.5	11.25	69	6C	5A	
19	Minimum Row Active to Row Active delay (tRRDmin) (ns)	7.5	6		3C	30		
20	Minimum row Precharge delay (tRPmin) (ns)	13.125	13.5	11.25	69	6C	5A	
21	Upper nibble for tRAS and tRC	1,1			11			
22	Minimum Active-to-Precharge delay (tRASmin) (ns)	37.5	36	35	2C	20	18	
23	Minimum Active-to-Active/Refresh delay (tRCmin) (ns)	50.625	49.5	46.25	95	8C	72	
24	Minimum refresh recovery delay (tRFCmin) LSB	(Combo bytes 24,25)			70			
25	Minimum refresh recovery delay (tRFCmin) MSB	110ns			03			
26	Minimum internal Write-to-Read command delay (tWTRmin)	7.5ns			3C			
27	Minimum internal Read-to-Precharge command delay (tRTPmin)	7.5ns			3C			
28	Minimum four active window delay (tFAWmin) LSB	(Combo byte 28, 29)			01	00		
29	Minimum four active window delay (tFAWmin) MSB	37.5ns	30ns		2C	F0		
30	SDRAM device output drivers suported	RZQ / 6,RZQ / 7, DLL-Off Mode Support,			83			
31	SDRAM device thermal and refresh options	Extended Temperature Range, ASR, ODTS, PASR,			8D			
32	Module thermal sensor	Non Thermal Sensor Support			--			
33	SDRAM device type	height ≦ 15mm			0F			
34-59	Reserved	thickness ≤ 1 mm			11			
60	Module height (nominal)	Raw Card A			00			

Serial Presence Detect -- Part 2 of 2 (1GB)

128Mx64 1 Rank UNBUFFERED DDR3 SDRAM DIMM based on 128Mx8, 8Banks, 8K Refresh, 1.5V DDR3 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		-BE	-CG	-DG	-BE	-CG	-DG	
61	Module thickness (Max)	Standard			00			
62	Raw Card ID reference	Undefined			--			
63	DRAM address mapping edge connector	Nanya Technology			830B			
64-116	Reserved	Undefined			00			
117-118	Module manufacture ID	Undefined			00			
119-125	Module information	Undefined			00			
126-127	CRC	Undefined			00000000			
128-145	Module part number	Calculated Value			227A	F05C	E202	
146	Module die revision	ASCII values			--			
147	Module PCB revision	Undefined			00			
148-149	DRAM device manufacturer ID	Undefined			00			
150-175	Manufacturer reserved	Nanya Technology			830B			
176-255	Customer reserved	Undefined			--			

SPD Note

SPD Entry Value	Serial PD Data Entry (Hexadecimal)
M2F1G64CB88A4N-BE	4D3246314736344342383841344E2D424520
M2F1G64CB88A4N-CG	4D3246314736344342383841344E2D434720
M2F1G64CB88A4N-DG	4D3246314736344342383841344E2D444720

Serial Presence Detect -- Part 1 of 2 (2GB)

256Mx64 2 Ranks UNBUFFERED DDR3 SDRAM DIMM based on 128Mx8, 8Banks, 8K Refresh, 1.5V DDR3 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		-BE	-CG	-DG	-BE	-CG	-DG	
0	CRC range, EEPROM bytes, bytes used	CRC Covers Bytes: 0~116, Total SPD Bytes: 256, SPD Bytes Used: 176,			92			
1	SPD revision	Revision 0.8			08			
2	DRAM device type	DDR3 SDRAM			0B			
3	Module type (form factor)	UDIMM			02			
4	SDRAM Device density and banks	8 banks, 1Gb			02			
5	SDRAM device row and column count	14 rows, 10 columns			11			
6	Reserved	Undefined			00			
7	Module ranks and device DQ count	2 ranks, 8 bits			09			
8	ECC tag and module memory Bus width	Non ECC, 64bits			03			
9	Fine timebase dividend/divisor (in ps)	2.5ps			52			
10	Medium timebase dividend	1ns			01			
11	Medium timebase divisor	8ns			08			
12	Minimum SDRAM cycle time (tCKmin) (ns)	1.875	1.5	1.25	0F	0C	0A	
13	Reserved	Undefined			00			
14	CAS latencies supported	6,7,8	6,8,9	5,6,7,8,9,10	1C	34	7E	
15	CAS latencies supported	Undefined			00			
16	Minimum CAS latency time (tAAmin) (ns)	13.125	13.5	11.25	69	6C	5A	
17	Minimum write recovery time (tWRmin)	15ns			78			
18	Minimum $\overline{CAS}$-to-$\overline{CAS}$ delay (tRCDmin) (ns)	13.125	13.5	11.25	69	6C	5A	
19	Minimum Row Active to Row Active delay (tRRDmin) (ns)	7.5	6		3C	30		
20	Minimum row Precharge delay (tRPmin) (ns)	13.125	13.5	11.25	69	6C	5A	
21	Upper nibble for tRAS and tRC	1,1			11			
22	Minimum Active-to-Precharge delay (tRASmin) (ns)	37.5	36	35	2C	20	18	
23	Minimum Active-to-Active/Refresh delay (tRCmin) (ns)	50.625	49.5	46.25	95	8C	72	
24	Minimum refresh recovery delay (tRFCmin) LSB	(Combo bytes 24,25)			70			
25	Minimum refresh recovery delay (tRFCmin) MSB	110ns			03			
26	Minimum internal Write-to-Read command delay (tWTRmin)	7.5ns			3C			
27	Minimum internal Read-to-Precharge command delay (tRTPmin)	7.5ns			3C			
28	Minimum four active window delay (tFAWmin) LSB	(Combo byte 28, 29)			01	00		
29	Minimum four active window delay (tFAWmin) MSB	37.5ns	30ns		2C	F0		
30	SDRAM device output drivers suported	RZQ / 6,RZQ / 7, DLL-Off Mode Support,			83			
31	SDRAM device thermal and refresh options	Extended Temperature Range, ASR, ODTS, PASR,			8D			
32	Module thermal sensor	Non Thermal Sensor Support			--			
33	SDRAM device type	height ≦ 15mm			0F			
34-59	Reserved	thickness ≤ 1 mm			11			
60	Module height (nominal)	Raw Card B			01			

Serial Presence Detect -- Part 2 of 2 (2GB)

256Mx64 2 Ranks UNBUFFERED DDR3 SDRAM DIMM based on 128Mx8, 8Banks, 8K Refresh, 1.5V DDR3 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		-BE	-CG	-DG	-BE	-CG	-DG	
61	Module thickness (Max)	Standard			01			
62	Raw Card ID reference	Undefined			--			
63	DRAM address mapping edge connector	Nanya Technology			830B			
64-116	Reserved	Undefined			00			
117-118	Module manufacture ID	Undefined			00			
119-125	Module information	Undefined			00			
126-127	CRC	Undefined			00000000			
128-145	Module part number	Calculated Value			ABEF	79C9	6B97	
146	Module die revision	ASCII values			--			
147	Module PCB revision	Undefined			00			
148-149	DRAM device manufacturer ID	Undefined			00			
150-175	Manufacturer reserved	Nanya Technology			830B			
176-255	Customer reserved	Undefined			--			

SPD Note

SPD Entry Value	Serial PD Data Entry (Hexadecimal)
M2F1G64CB88A4N-BE	4D3246324736344342384841344E2D424520
M2F1G64CB88A4N-CG	4D3246324736344342384841344E2D434720
M2F1G64CB88A4N-DG	4D3246324736344342384841344E2D444720

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.4 to 1.975	V
V_{DD}	Voltage on VDD supply relative to Vss	-0.4 to 1.975	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.4 to 1.975	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics and Operating Conditions

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.5V ± 0.075V; V_{DD} = 1.5V ± 0.075V, See AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	1.425	1.575	V	1
V_{DDQ}	I/O Supply Voltage	1.425	1.575	V	1
V_{REF}	I/O Reference Voltage	0.49V_{DDQ}	0.51V_{DDQ}	V	1, 2

Note:
1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.

Environmental Parameters

Symbol	Parameter	Rating	Units	Note
T_{OPR}	Module Operating Temperature Range (ambient)	0 to 55	°C	3
H_{OPR}	Operating Humidity (relative)	10 to 90	%	1
T_{STG}	Storage Temperature (Plastic)	-50 to 100	°C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

Note:
1. Stresses greater than those listed may cause permanent damage to the device. This is a tress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The component maximum case temperature shall not exceed the value specified in the component spec.

Single Ended AC and DC Input Levels

Symbol	Parameter	DDR3-1066, DDR3-1333, DDR3-1600		Units	Note
		Min.	Max.		
VIH (DC)	DC input logic high	Vref + 0.100	VDD	V	1
VIL (DC)	DC input logic low	VSS	Vref – 0.100	V	1
VIH (AC)	AC input logic high	Vref + 0.175		V	1
VIL (AC)	AC input logic low	-	Vref – 0.175	V	1
VrefDQ(DC)	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	V	2,3
VrefCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	2,3

Note:
1. For DQ and DM, Vref = VrefDQ. For input only pins except $\overline{\text{RESET}}$, Vref = VrefCA.
2. The AC peak noise on Vref may not allow Vref to deviate from Vref(DC) by more than +/- 1% VDD.
3. For reference: approx. VDD/2 +/- 15mV.

Operating, Standby, and Refresh Currents

T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.5V ± 0.075V (1GB, 1 Rank, base on 128Mx8 DDR3 SDRAMs)

Symbol	Parameter/Condition	DDR3-1066	DDR3-1333	DDR3-1600	Unit
I_{DD0}	Operating Current: one bank activate/Precharge	TBD	TBD	TBD	mA
I_{DD1}	Operating Current: one bank activate/Read/Precharge	TBD	TBD	TBD	mA
$I_{DD2P(0)}$	Precharge Power-Down Current Fast Exit-MR0 bit A12=0	TBD	TBD	TBD	mA
$I_{DD2P(1)}$	Precharge Power Down Current Slow Exit-MR0 bit A12=1	TBD	TBD	TBD	mA
I_{DD2N}	Precharge Standby Current	TBD	TBD	TBD	mA
I_{DD2Q}	Precharge Quiet Standby current	TBD	TBD	TBD	mA
I_{DD3P}	Active Power-Down Current Always Fast Exit	TBD	TBD	TBD	mA
I_{DD3N}	Active Standby Current	TBD	TBD	TBD	mA
I_{DD4W}	Operating Current: Burst Write	TBD	TBD	TBD	mA
I_{DD4R}	Operating Current: Burst Read	TBD	TBD	TBD	mA
I_{DD5B}	Burst Refresh Current	TBD	TBD	TBD	mA
I_{DD6}	Self-Refresh Current Normal Temperature Range (0-85C)	TBD	TBD	TBD	mA
I_{DD6ET}	Self-Refresh Current Extended Temperature Range (0-95C)	TBD	TBD	TBD	mA
I_{DD7}	All Bank Interleave Read Current	TBD	TBD	TBD	mA
Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.					

Operating, Standby, and Refresh Currents

T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.5V ± 0.075V (2GB, 2 Ranks, base on 128Mx8 DDR3 SDRAMs)

Symbol	Parameter/Condition	DDR3-1066	DDR3-1333	DDR3-1600	Unit
I_{DD0}	Operating Current: one bank activate/Precharge	TBD	TBD	TBD	mA
I_{DD1}	Operating Current: one bank activate/Read/Precharge	TBD	TBD	TBD	mA
$I_{DD2P(0)}$	Precharge Power-Down Current Fast Exit-MR0 bit A12=0	TBD	TBD	TBD	mA
$I_{DD2P(1)}$	Precharge Power Down Current Slow Exit-MR0 bit A12=1	TBD	TBD	TBD	mA
I_{DD2N}	Precharge Standby Current	TBD	TBD	TBD	mA
I_{DD2Q}	Precharge Quiet Standby current	TBD	TBD	TBD	mA
I_{DD3P}	Active Power-Down Current Always Fast Exit	TBD	TBD	TBD	mA
I_{DD3N}	Active Standby Current	TBD	TBD	TBD	mA
I_{DD4W}	Operating Current: Burst Write	TBD	TBD	TBD	mA
I_{DD4R}	Operating Current: Burst Read	TBD	TBD	TBD	mA
I_{DD5B}	Burst Refresh Current	TBD	TBD	TBD	mA
I_{DD6}	Self-Refresh Current Normal Temperature Range (0-85C)	TBD	TBD	TBD	mA
I_{DD6ET}	Self-Refresh Current Extended Temperature Range (0-95C)	TBD	TBD	TBD	mA
I_{DD7}	All Bank Interleave Read Current	TBD	TBD	TBD	mA
Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.					

Speed Bins

Speed Bin			DDR3-1066 (-BE)		DDR3-1333 (-CG)		DDR3-1600(-DG)		Unit
CL - nRCD - nRP			7-7-7		9-9-9		9-9-9		
Parameter		Symbol	Min	Max	Min	Max	Min	Max	
Internal read command to first data		tAA	13.125	20	13.5	20	11.25	20	ns
ACT to internal read or write delay time		tRCD	13.125	--	13.5	--	11.25	--	ns
PRE command period		tRP	13.125	--	13.5	--	11.25	--	ns
ACT to ACT or REF command period		tRC	50.625	--	49.5	--	46.25	--	ns
ACT to PRE command period		tRAS	37.5	9*tREFI	36	9*tREFI	35	9*tREFI	ns
CL = 5	CWL=5	tCK(AVG)	Reserved		Reserved		2.5	3.3	ns
	CWL=6, 7, 8	tCK(AVG)	Reserved		Reserved		Reserved		ns
CL = 6	CWL=5	tCK(AVG)	2.5	3.3	2.5	3.3	2.5	3.3	ns
	CWL=6	tCK(AVG)	Reserved		Reserved		1.875	<2.5	ns
	CWL=7, 8	tCK(AVG)	Reserved		Reserved		Reserved		ns
CL = 7	CWL=5	tCK(AVG)	Reserved		Reserved		Reserved		ns
	CWL=6	tCK(AVG)	1.875	<2.5	Reserved		1.875	<2.5	ns
	CWL=7	tCK(AVG)	Reserved		Reserved		Reserved		ns
	CWL=8	tCK(AVG)	Reserved		Reserved		Reserved		ns
CL = 8	CWL=5	tCK(AVG)	Reserved		Reserved		Reserved		ns
	CWL=6	tCK(AVG)	1.875	<2.5	1.875	<2.5	1.875	<2.5	ns
	CWL=7	tCK(AVG)	Reserved		Reserved		1.5	<1.875	ns
	CWL=8	tCK(AVG)	Reserved		Reserved		Reserved		ns
CL = 9	CWL=5, 6	tCK(AVG)	Reserved		Reserved		Reserved		ns
	CWL=7	tCK(AVG)	Reserved		1.5	<1.875	1.5	<1.875	ns
	CWL=8	tCK(AVG)	Reserved		Reserved		1.25	<1.5	ns
Supported CL settings			6,7,8		6,8,9		5,6,7,8,9,10		nCK
Supported CWL Settings			5,6		5,6,7		5,6,7,8		nCK

AC Timing Specifications for DDR3 SDRAM Devices Used on Module

		DDR3-1066		DDR3-1333		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**
Clock Timing						
Minimum Clock Cycle time (DLL off mode)	tCK(DLL_OFF)	8	-	8		ns
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg)min +tJIT(per)min	tCK(avg)max +tJIT(per)max	tCK(avg)min +tJIT(per)min	tCK(avg)max +tJIT(per)max	ps
Absolute clock high pulse width	tCH(abs)	0.43	-	0.43	-	ps
Absolute clock low pulse width	tCL(abs)	0.43	-	0.43	-	ps
Clock Period Jitter	tJIT(per)	-90	90	-80	80	ps
Clock Period Jitter during DLL locking period	tJIT(per,lck)	-80	80	-70	70	ps
Cycle to Cycle Period Jitter	tJIT(cc)	180		160		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc,lck)	160		140		ps
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	ps
Cumulative error across 2 cycles	tERR(2per)	-132	132	-118	118	ps
Cumulative error across 3 cycles	tERR(3per)	-157	157	-140	140	ps
Cumulative error across 4 cycles	tERR(4per)	-175	175	-155	155	ps
Cumulative error across 5 cycles	tERR(5per)	-188	188	-168	168	ps
Cumulative error across 6 cycles	tERR(6per)	-200	200	-177	177	ps
Cumulative error across 7 cycles	tERR(7per)	-209	209	-186	186	ps
Cumulative error across 8 cycles	tERR(8per)	-217	217	-193	193	ps
Cumulative error across 9 cycles	tERR(9per)	-224	224	-200	200	ps
Cumulative error across 10 cycles	tERR(10per)	-231	231	-205	205	ps
Cumulative error across n=11~50 cycles	tERR(nper)	tERR(npr)min =(1+0.68ln(n))*tJIT (per)min	tERR(npr)max =(1+0.68ln(n))*tJIT (per)max	tERR(npr)min =(1+0.68ln(n))*tJIT (per)min	tERR(npr)max =(1+0.68ln(n))*tJIT (per)max	ps
Data Timing						
DQS, $\overline{DQS}$ to DQ skew, per group, per access	tDQSQ	-	150		125	ps
DQ output hold time from DQS, $\overline{DQS}$	tQH	0.38	-	0.38		tCK(avg)
DQ low-impedance time from CK, $\overline{CK}$	tLZ(DQ)	-600	300	-500	250	ps
DQ high-impedance time from CK, $\overline{CK}$	tHZ(DQ)	-	300		250	ps
Data setup time to DQS, DQS reference to Vih(ac) / Vil(ac) levels	tDS(base)	25		TBD		ps
Data hold time to DQS, DQS reference to Vih(ac) / Vil(ac) levels	tDH(base)	100		TBD		ps
Data Strobe Timing						
DQS, $\overline{DQS}$ differential READ Preamble	tRPRE	0.9	-	0.9	-	tCK(avg)
DQS, $\overline{DQS}$ differential READ Postamble	tRPST	0.3	-	0.3	-	tCK(avg)
DQS, $\overline{DQS}$ differential output high time	tQSH	0.38	-	0.40		tCK(avg)
DQS, $\overline{DQS}$ differential output low time	tQSL	0.38	-	0.40		tCK(avg)
DQS, $\overline{DQS}$ differential WRITE Preamble	tWPRE	0.9	-	0.9		tCK(avg)
DQS, $\overline{DQS}$ differential WRITE Postamble	tWPST	0.3	-	0.3		tCK(avg)
DQS, $\overline{DQS}$ rising dege output access time from rising CK, $\overline{CK}$	tDQSCK	-300	300	-255	255	ps
DQS, $\overline{DQS}$ low-impedance time (Reference from RL-1)	tLZ(DQS)	-600	300	-500	250	ps
DQS, $\overline{DQS}$ high-impedance time (Reference from RL + BL/2)	tHZ(DQS)	-	300		250	ps
DQS, $\overline{DQS}$ differential input low pulse width	tDQSL	0.4	0.6	0.4	0.6	tCK(avg)
DQS, $\overline{DQS}$ differential input high pulse width	tDQSH	0.4	0.6	0.4	0.6	tCK(avg)
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	tDQSS	-0.25	0.25	-0.25	0.25	tCK(avg)
DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge	tDSS	0.2	-	0.2	-	tCK(avg)
DQS, $\overline{DQS}$ falling edge hold time to CK, $\overline{CK}$ rising edge	tDSH	0.2	-	0.2	-	tCK(avg)

Parameter	Symbol	DDR3-1066 Min	DDR3-1066 Max	DDR3-1333 Min	DDR3-1333 Max	Units
Command and Address Timing						
DLL locking time	tDLLK	512	-	512	-	nCK
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	
WRITE recovery time	tWR	15	-	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	4	-	nCK
Mode Register Set command update delay	tMOD	max(12nCK, 15ns)	-	max(12nCK, 15ns)	-	
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	4	-	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP/tCK(avg))				nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4nCK, 7.5ns)	-	max(4nCK, 6ns)	-	
Four activate window for 1KB page size	tFAW	37.5	-	30	-	ns
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	tIS(base)	125	-	65	-	ps
Command and Address hold time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	tIH(base)	200	-	140	-	ps
Calibrating Timing						
Power-up and RESET calibration time	tZQinit	512	-	512	-	nCK
Normal operation Full calibration time	tZQoper	256	-	256	-	nCK
Normal operation Short calibration time	tZQCS	64	-	64	-	nCK
Reset Timing						
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	
Self Refresh Timings						
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	nCK
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKE(min) + 1nCK	-	tCKE(min) + 1nCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	
Valid Clock Requirement after Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	
Power Down Timings						
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nCK, 7.5ns)	-	max(3nCK, 6ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10nCK, 24ns)	-	max(10nCK, 24ns)	-	
CKE minimum pulse width	tCKE	max(3nCK, 5.625ns)	-	max(3nCK, 5.625ns)	-	
Command pass disable delay	tCPDED	1	-	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL+2+WR+1	-	WL+2+WR+1	-	nCK
Timing of REF command to Power down entry	tREFPDEN	1	-	1	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	

		DDR3-1066		DDR3-1333		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**
ODT Timings						
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	6	-	nCK
Asynchronous RTT turn-on delay (Power - Down with DLL frozen)	tAONPD	1	9	1	9	ns
Asynchronous RTT turn-off delay (Power – Down with DLL frozen)	tAOFPD	1	9	1	9	ns
RTT turn-on	tAON	-300	300	-250	250	ps
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	tCK(avg)
Write Leveling Timings						
First DQS/$\overline{DQS}$ rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	nCK
DQS/DQS delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	nCK
Write leveling setup time from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing	tWLS	245	-	195	-	ps
Write leveling setup hold from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing	tWLH	245	-	195	-	ps
Write leveling output delay	tWLO	0	9	0	9	ns
Write leveling output error	tWLOE	0	2	0	2	ns

AC Timing Specifications for DDR3 SDRAM Devices Used on Module

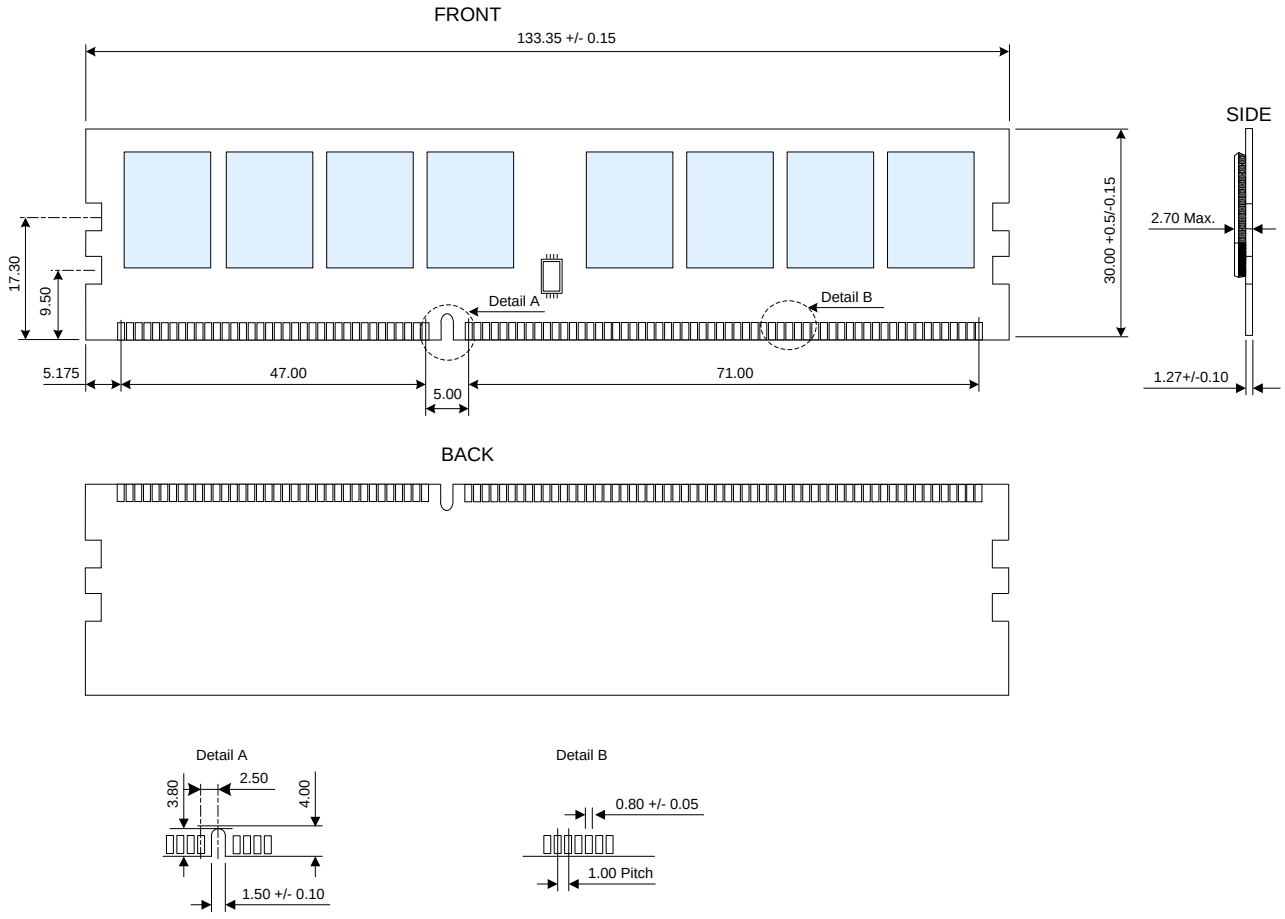
		DDR3-1600		
Parameter	**Symbol**	**Min**	**Max**	**Units**
Clock Timing				
Minimum Clock Cycle time (DLL off mode)	tCK(DLL_OFF)	8	-	ns
Average high pulse width	tCH(avg)	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max +tJIT(per)max	ps
Absolute clock high pulse width	tCH(abs)	0.43	-	ps
Absolute clock low pulse width	tCL(abs)	0.43	-	ps
Clock Period Jitter	tJIT(per)	-70	70	ps
Clock Period Jitter during DLL locking period	tJIT(per,lck)	-60	60	ps
Cycle to Cycle Period Jitter	tJIT(cc)	140		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc,lck)	120		ps
Duty Cycle Jitter	tJIT(duty)	-	-	ps
Cumulative error across 2 cycles	tERR(2per)	-103	103	ps
Cumulative error across 3 cycles	tERR(3per)	-122	122	ps
Cumulative error across 4 cycles	tERR(4per)	-136	136	ps
Cumulative error across 5 cycles	tERR(5per)	-147	147	ps
Cumulative error across 6 cycles	tERR(6per)	-155	155	ps
Cumulative error across 7 cycles	tERR(7per)	-163	163	ps
Cumulative error across 8 cycles	tERR(8per)	-169	169	ps
Cumulative error across 9 cycles	tERR(9per)	-175	175	ps
Cumulative error across 10 cycles	tERR(10per)	-180	180	ps
Cumulative error across n=11~50 cycles	tERR(nper)	tERR(npr)min =(1+ 0.68ln(n))*tJIT(per)min	tERR(npr)max =(1+ 0.68ln(n))*tJIT(per)max	ps
Data Timing				
DQS, $\overline{DQS}$ to DQ skew, per group, per access	tDQSQ	-	100	ps
DQ output hold time from DQS, $\overline{DQS}$	tQH	0.38	-	tCK(avg)
DQ low-impedance time from CK, $\overline{CK}$	tLZ(DQ)	-450	225	ps
DQ high-impedance time from CK, $\overline{CK}$	tHZ(DQ)	-	225	ps
Data setup time to DQS, DQS reference to Vih(ac) / Vil(ac) levels	tDS(base)	TBD		ps
Data hold time to DQS, DQS reference to Vih(ac) / Vil(ac) levels	tDH(base)	TBD		ps
Data Strobe Timing				
DQS, $\overline{DQS}$ differential READ Preamble	tRPRE	0.9	-	tCK(avg)
DQS, $\overline{DQS}$ differential READ Postamble	tRPST	0.3	-	tCK(avg)
DQS, $\overline{DQS}$ differential output high time	tQSH	0.40	-	tCK(avg)
DQS, $\overline{DQS}$ differential output low time	tQSL	0.40	-	tCK(avg)
DQS, $\overline{DQS}$ differential WRITE Preamble	tWPRE	0.9	-	tCK(avg)
DQS, $\overline{DQS}$ differential WRITE Postamble	tWPST	0.3	-	tCK(avg)
DQS, $\overline{DQS}$ rising dege output access time from rising CK, $\overline{CK}$	tDQSCK	-225	225	ps
DQS, $\overline{DQS}$ low-impedance time (Reference from RL-1)	tLZ(DQS)	-450	225	ps
DQS, $\overline{DQS}$ high-impedance time (Reference from RL + BL/2)	tHZ(DQS)	-	225	ps
DQS, $\overline{DQS}$ differential input low pulse width	tDQSL	0.4	0.6	tCK(avg)
DQS, $\overline{DQS}$ differential input high pulse width	tDQSH	0.4	0.6	tCK(avg)
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	tDQSS	-0.25	0.25	tCK(avg)
DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge	tDSS	0.2	-	tCK(avg)
DQS, $\overline{DQS}$ falling edge hold time to CK, $\overline{CK}$ rising edge	tDSH	0.2	-	tCK(avg)

		DDR3-1600		
Parameter	**Symbol**	**Min**	**Max**	**Units**
Command and Address Timing				
DLL locking time	tDLLK	512	-	nCK
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max(4nCK, 7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	nCK
Mode Register Set command update delay	tMOD	max(12nCK, 15ns)	-	
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP/tCK(avg))		nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4nCK, 6ns)	-	
Four activate window for 2KB page size	tFAW	30	-	ns
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	tIS(base)	TBD	-	ps
Command and Address hold time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	tIH(base)	TBD	-	ps
Calibrating Timing				
Power-up and RESET calibration time	tZQinit	512	-	nCK
Normal operation Full calibration time	tZQoper	256	-	nCK
Normal operation Short calibration time	tZQCS	64	-	nCK
Reset Timing				
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC(min) + 10ns)	-	
Self Refresh Timings				
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC(min) + 10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKE(min) + 1nCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	
Valid Clock Requirement after Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	
Power Down Timings				
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nCK, 6ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10nCK, 24ns)	-	
CKE minimum pulse width	tCKE	max(3nCK, 5ns)	-	
Command pass disable delay	tCPDED	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	1	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL+2+(tWR/tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL+2+WR+1	-	nCK
Timing of REF command to Power down entry	tREFPDEN	1	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	

		DDR3-1600		
Parameter	**Symbol**	**Min**	**Max**	**Units**
ODT Timings				
ODT high time without write command or with write command and BC4	ODTH4	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	nCK
Asynchronous RTT turn-on delay (Power - Down with DLL frozen)	tAONPD	1	9	ns
Asynchronous RTT turn-off delay (Power – Down with DLL frozen)	tAOFPD	1	9	ns
RTT turn-on	tAON	-225	225	ps
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)
Write Leveling Timings				
First DQS/$\overline{\text{DQS}}$ rising edge after write leveling mode is programmed	tWLMRD	40	-	nCK
DQS/DQS delay after write leveling mode is programmed	tWLDQSEN	25	-	nCK
Write leveling setup time from rising CK, $\overline{\text{CK}}$ crossing to rising DQS, $\overline{\text{DQS}}$ crossing	tWLS	TBD	-	ps
Write leveling setup hold from rising CK, $\overline{\text{CK}}$ crossing to rising DQS, $\overline{\text{DQS}}$ crossing	tWLH	TBD	-	ps
Write leveling output delay	tWLO	0	7.5	ns
Write leveling output error	tWLOE	0	2	ns

Package Dimensions

(1GB, 1 Rank, 128Mx8 DDR3 SDRAMs)

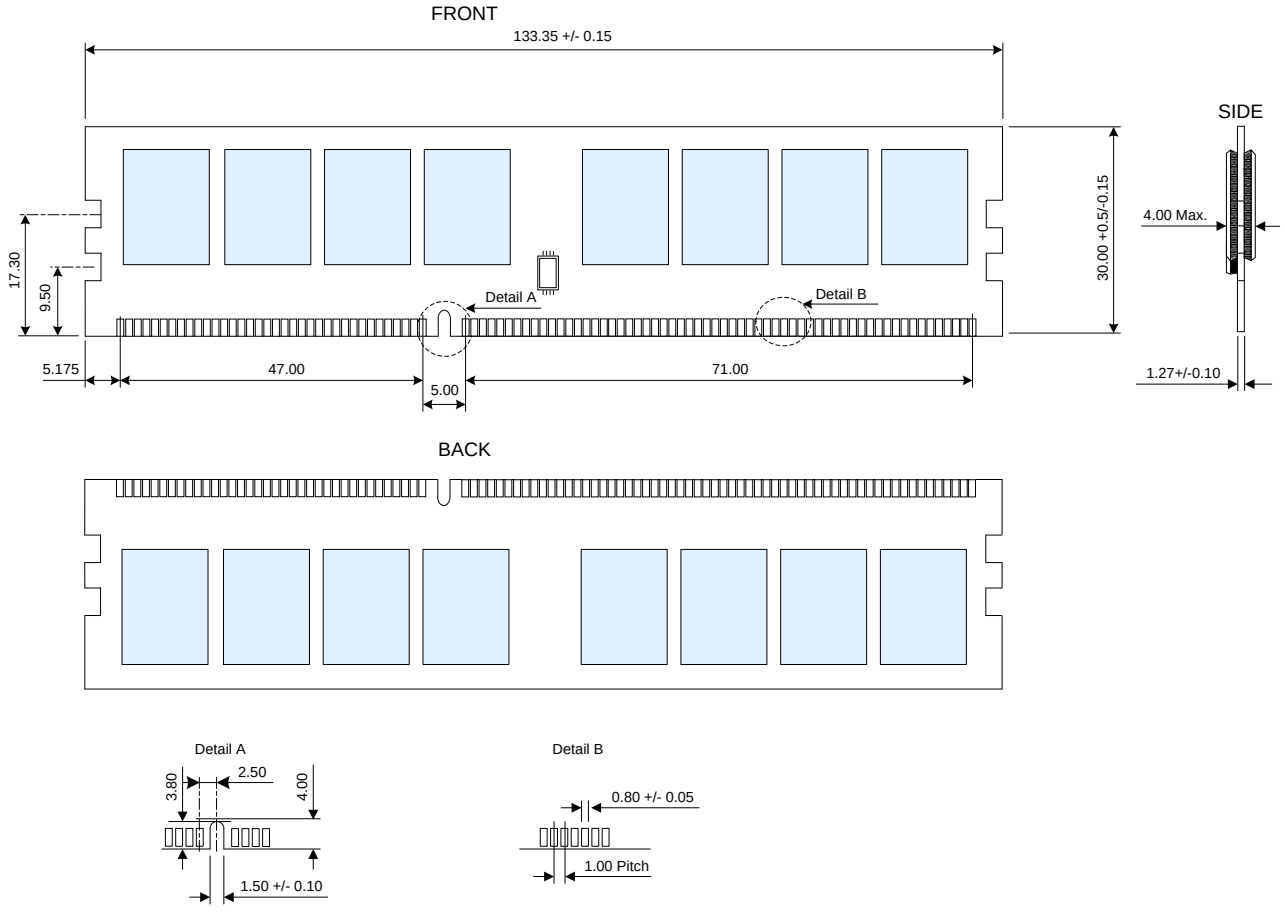


Units: Millimeters

Note: Device position is only for reference.

Package Dimensions

(2GB, 2 Ranks, 128Mx8 DDR3 SDRAMs)



Units: Millimeters

Note: Device position is only for reference.

Revision Log

Rev	Date	Modification
0.1	06/2008	Preliminary Edition